



## Description

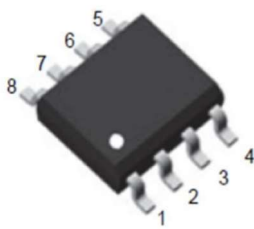
### JMT N-channel Enhancement Mode Power MOSFET

#### Features

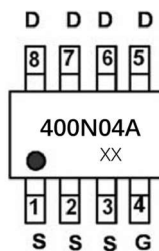
- 40V, 6A  
 $R_{DS(ON)} < 37m\Omega @ V_{GS} = 10V$   
 $R_{DS(ON)} < 52m\Omega @ V_{GS} = 4.5V$
- Lead free and Green Device Available
- Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead free product is acquired

#### Application

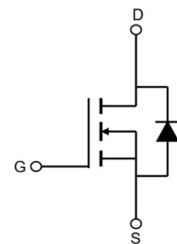
- Load Switch
- PWM Application
- Power management



SOP-8 top view



Marking and pin Assignment



Schematic Diagram

## Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
400N04A	JMTP400N04A	TAPING	SOP-8	13inch	4000	48000

## Absolute Maximum Ratings (T<sub>A</sub>=25°C unless otherwise specified)

Symbol	Parameter	Max.	Units
V <sub>DSS</sub>	Drain-Source Voltage	40	V
V <sub>GSS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Continuous Drain Current	T <sub>A</sub> = 25°C	6
		T <sub>A</sub> = 100°C	4
I <sub>DM</sub>	Pulsed Drain Current <sup>note1</sup>	24	A
P <sub>D</sub>	Power Dissipation	T <sub>A</sub> = 25°C	2.3
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient	54.3	°C/W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150	°C



## Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristic</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	40	-	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V,	-	-	1.0	μA
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V	-	-	±100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.5	2.2	V
R <sub>DS(on)</sub>	Static Drain-Source on-Resistance <small>note3</small>	V <sub>GS</sub> =10V, I <sub>D</sub> =4A	-	28	37	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =3A	-	37	52	
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, f=1.0MHz	-	435	-	pF
C <sub>oss</sub>	Output Capacitance		-	58	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	35	-	pF
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =20V, I <sub>D</sub> =3A, V <sub>GS</sub> =10V	-	11	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	2	-	nC
Q <sub>gd</sub>	Gate-Drain("Miller") Charge		-	2.5	-	nC
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> =20V, I <sub>D</sub> =4A, R <sub>L</sub> =1Ω, R <sub>GEN</sub> =3Ω, V <sub>GS</sub> =10V	-	10	-	ns
t <sub>r</sub>	Turn-on Rise Time		-	8	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time		-	29	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	12	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	6	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	24	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =6A	-	-	1.2	V
t <sub>rr</sub>	Body Diode Reverse Recovery Time	T <sub>J</sub> =25°C, I <sub>F</sub> =6A, dI/dt=100A/μs	-	20	-	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge		-	11	-	nC

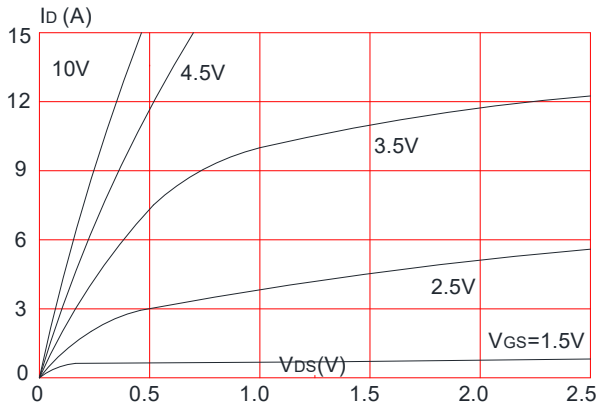
Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

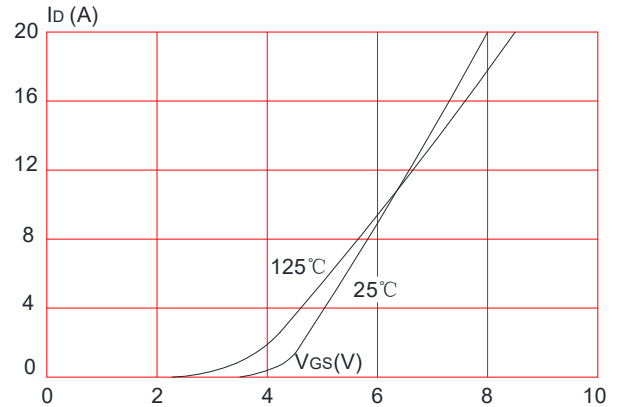


## Typical Performance Characteristics

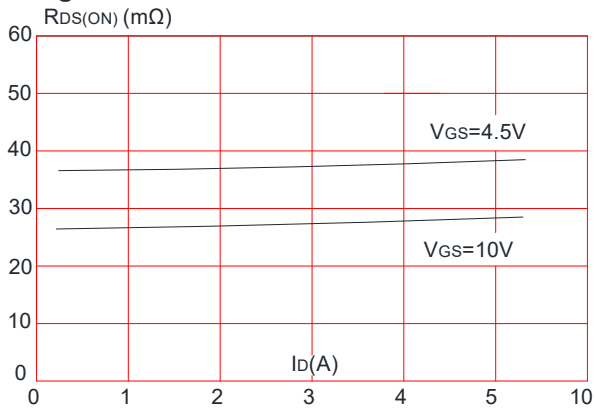
**Figure 1:** Output Characteristics



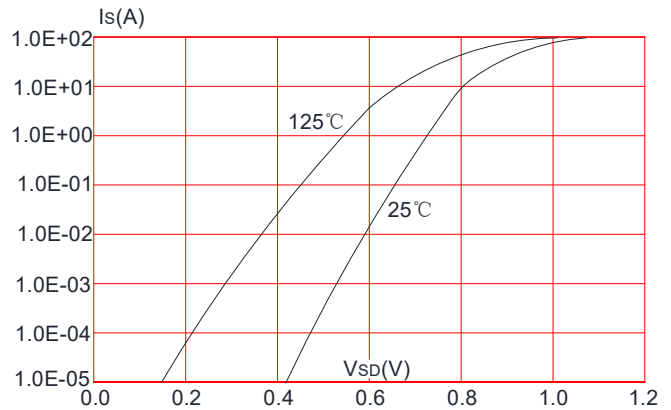
**Figure 2:** Typical Transfer Characteristics



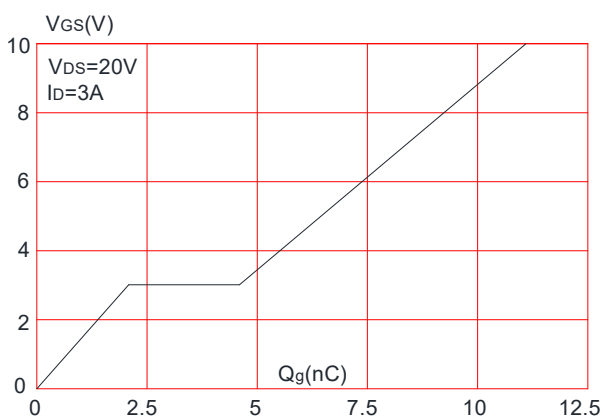
**Figure 3:** On-resistance vs. Drain Current



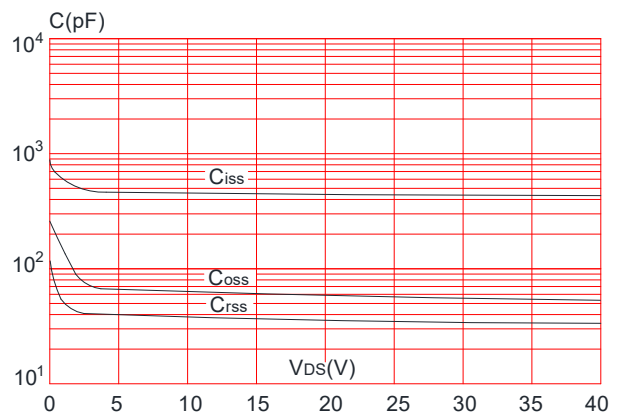
**Figure 4:** Body Diode Characteristics



**Figure 5:** Gate Charge Characteristics

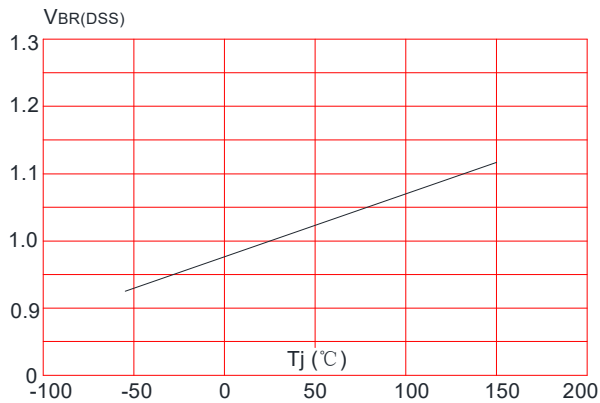


**Figure 6:** Capacitance Characteristics

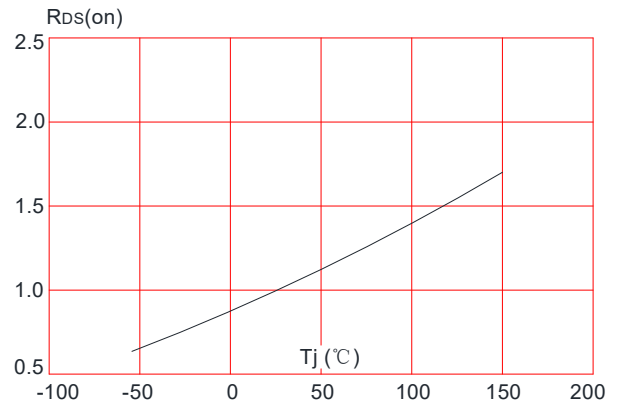




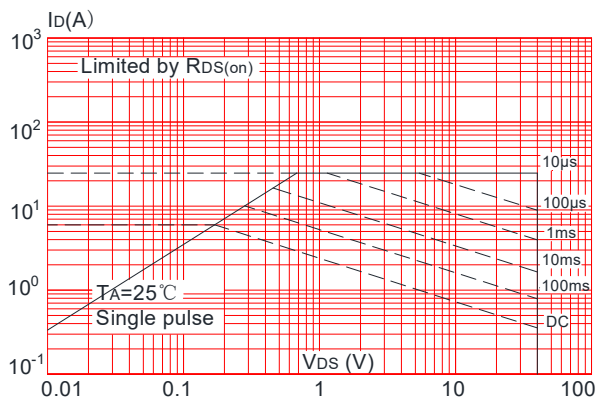
**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature



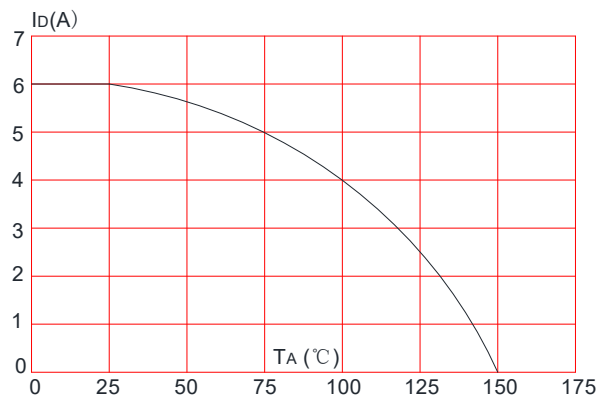
**Figure 8:** Normalized on Resistance vs. Junction Temperature



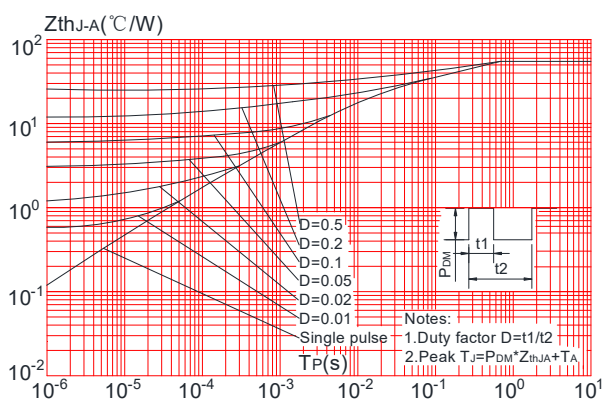
**Figure 9:** Maximum Safe Operating Area



**Figure 10:** Maximum Continuous Drain Current vs. Ambient Temperature



**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



## Test Circuit



Figure 1: Gate Charge Test Circuit & Waveform

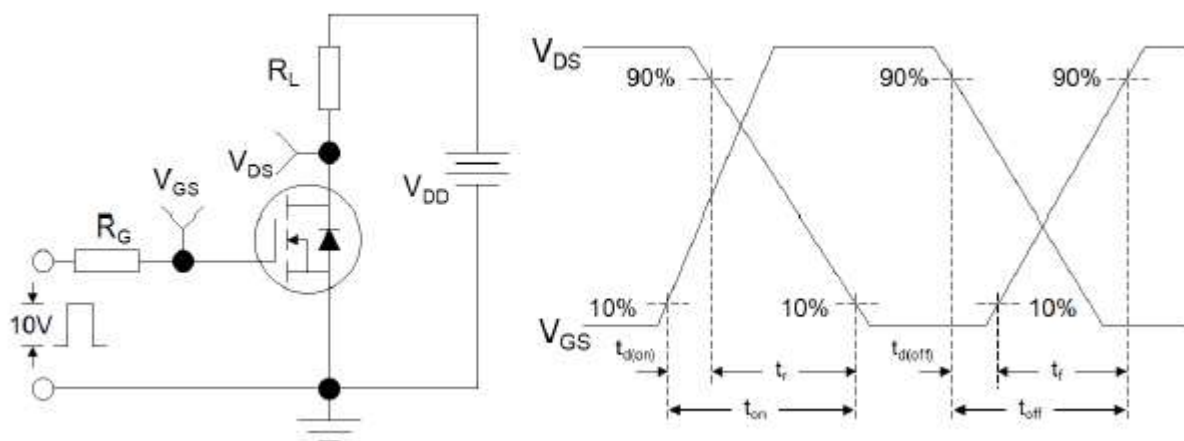


Figure 2: Resistive Switching Test Circuit & Waveforms

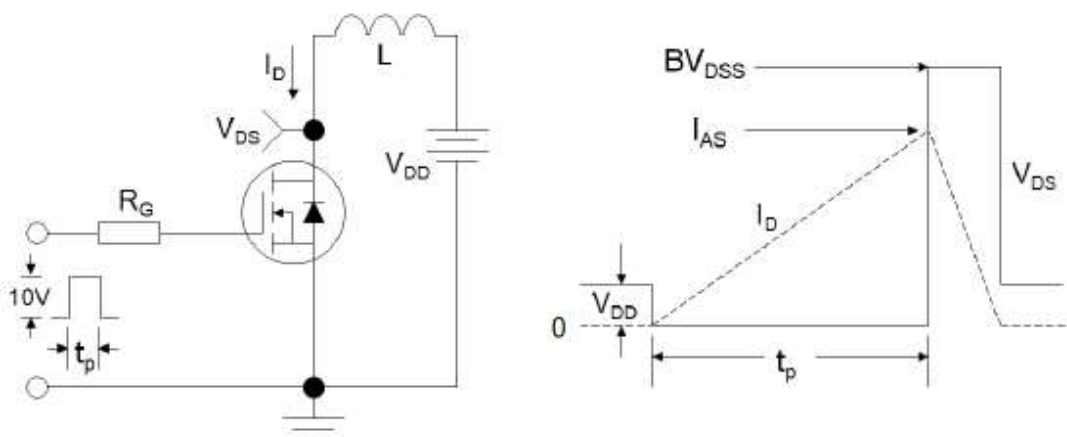
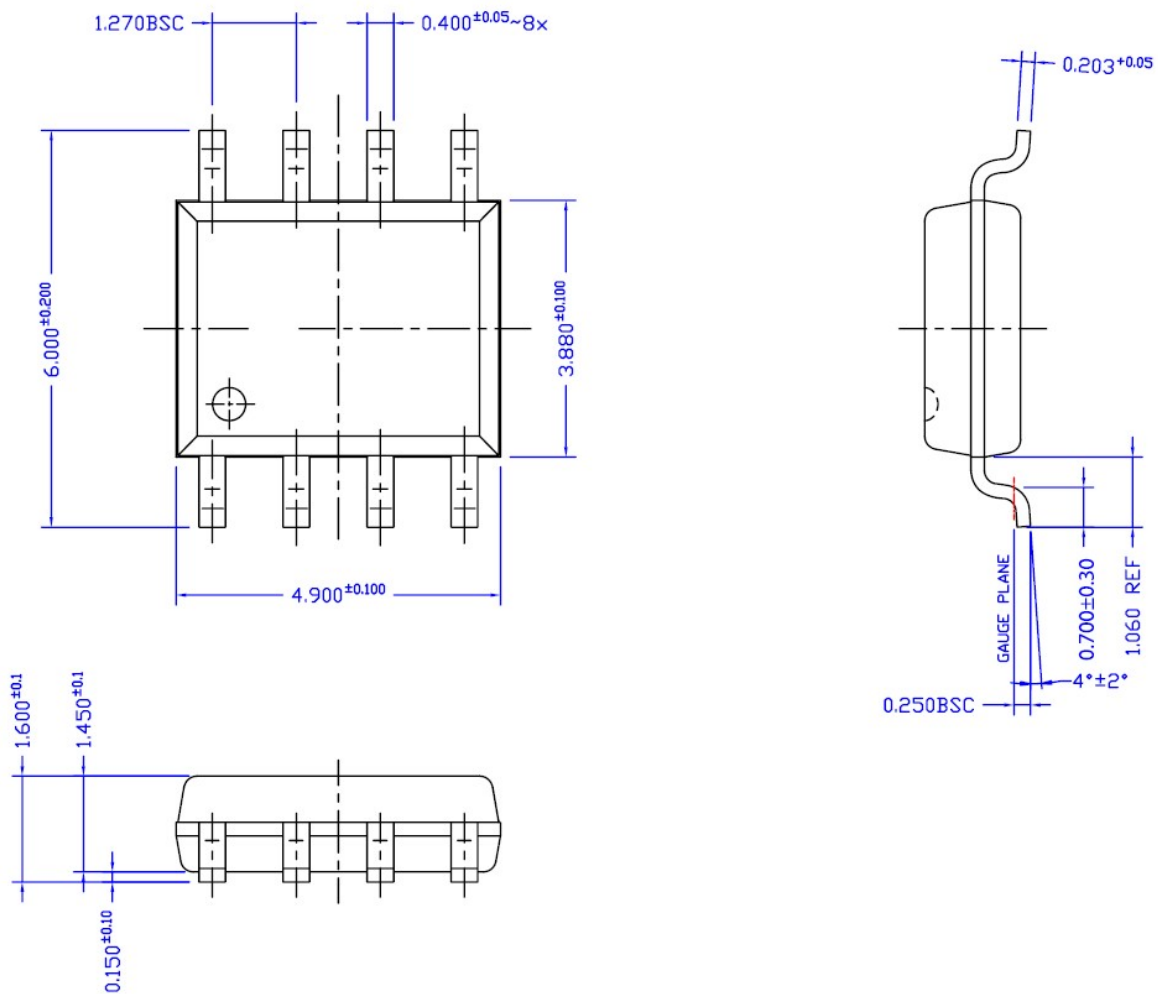


Figure 3: Unclamped Inductive Switching Test Circuit & Waveforms



## Package Mechanical Data-SOP-8



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